IBM's sGe works with high-K

IBM has demonstrated a technique that triples the performance of a standard transistor by a CMOS compatible process to achieving continued performance enhancement of chips and the electronic systems. This involves creating of a layer of strained germanium in the chanel of the transistor through which electrical current flows. Germanium has better conductivity than silicon, and the strain in the germanium layer created by IBM's process leads to further performance gains.

The concept of enhancing circuit performance by boosting the transistors' current transport properties using strained silicon, is in production by several companies today. However, IBM has demonstrated methods that can selectively place the sGe on the selected areas of a chip using a CMOS-compatible process.

The introduction of germanium in the critical areas of the IC provides an alternative means of improving chip performance from simply shrinking circuitry, increasingly important as further miniaturisation becomes more difficult and yields diminishing returns. IBM believes this could help ensure continued performance improvements in chips with circuit sizes of 32nm circuits and smaller.

"With this work we've drawn from our experience introducing technologies like SiGe, SOI and sSi. Our focus is on the application of that learning to develop innovative solutions for our customers," says T C Chen, IBM Fellow and VP of Science and Technology, IBM Research.

The selective introduction of sGe only in the critical areas of the integrated circuit provides a transistor with three times the performance without affecting other devices or circuits on the same chip. This dramatically reduces the risk of introducing a new material.

Within the transistor itself, IBM's selective sGe technique introduces other fringe benefits. For example, the industry is looking for solutions to replace conventional SiO_2 gate oxide using 'high-K' insulators, challenging for silicon. In contrast, the electrical properties of the sGe provides an easier way to introduce 'high-K' insulators.

Smoothing out silicon

IQE plc offers strained silicon technology that potentially opens the way for more rapid deployment of this leading edge technology within the semiconductor industry. Initial device results obtained on UltraSmooth Strained silicon product range, demonstrate a significant enhancement in speed for both nMOS and pMOS devices at sub 100nm indicating that the smoother surfaces leads directly to better pMOS performance.

Enhancement to pMOS devices was previously understood to come about only through introduction of even higher levels of strain by increasing the proportion of germanium in theSiGe buffer layer. However, increased strain results in greater distortion and increased defect levels and an accompanying adverse effect on both nMOS and pMOS device performance.

IQE's approach, for which patent applications have been filed, has been to concentrate on a simple, cost effective, single-stage epitaxial process to produce very low dislocation levels with an "UltraSmooth" strained silicon surface finish. After working closely with a major silicon IC manufacturer to assess device performance, results show that significant enhancements to both p-type and n-type devices can be achieved for sSi with buffer layers of Ge concentrations as low as 17%.

The high quality of the strained silicon material and performance have been confirmed by a number of other major chip manufacturers in Europe, North America and the Far East with whom IQE has been working during the last 12 months. Extensive testing and measurement demonstrate that IQE's 17% strained silicon exhibited improvements in mobility (speed) of up to 100% for the nMOS and up to 15% for the pMOS.

The mobility enhancement of nMOS and pMOS performance is of particular significance, since it should enable the more rapid commercial adoption of strained silicon technology and the scope of IQE's patent applications covers all key processes for carrier enhancement by the reduction of surface roughness on any form of strained silicon including strained silicon on insulator (sSOI).

Silicon rectifiers outperform SiC technology

Three new dual high-voltage Schottky rectifiers are offered by Vishay Intertechnology Inc. It claims these devices offer a 200V reverse voltage, which is said to be the highest available voltage for a silicon Schottky rectifier, a 20A forward current rating, and a maximum operating junction temperature of 175°C.

In fact, the new products are touted by the company to outperform 200V forward voltage Schottky rectifiers built on SiC technology at a fraction of the cost.

Designed for secondary rectification of ac-to-dc and dc-to-dc converters with outputs up to 48V, as well as freewheeling and polarity protection applications, With a typical forward voltage drop of 0.65V at 10A and 125°C, small 1mA maximum reverse leakage current at 125°C, and a 290A forward surge current per leg, these devices have been optimized for 50W to 250W power supply applications.

In addition, they feature a large peak non-repetitive reverse surge energy of 20mJ at 8/20µs per leg, and provide a negligible reverse recovery time, which, combined with their low forward voltage, improves power efficiency and reduces heat in end products.

All three devices feature a dual chip, common cathode configuration and maximum operating junction temperature of 175°C. Packaging options include TO-220AB (MBR20H200CT), isolated TO-220AB (MBRF20H200CT) and TO-262AA (MBRB20H200CT-1).

Samples and production quantities of the new Schottky rectifiers are already available, with lead times of six weeks for larger orders.